

High-Efficiency GaInP/GaAs HBT MMIC Power Amplifier with up to 9 W Output Power at 10 GHz

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Abstract—Monolithic power amplifiers using adequately ballasted high-efficiency GaInP/GaAs heterojunction bipolar transistors (HBT's) have been designed, fabricated, and tested. A maximum output power of 9 W with a power-added efficiency (PAE) of 42% and peak power-added efficiencies of 45% have been achieved at 10 GHz under critical long pulse conditions (pulse width = 100 μ s, duty cycle = 10%). To our knowledge these results represent the best performance of any GaInP/GaAs HBT MMIC power amplifier considering efficiency, output power, operation frequency, and pulse conditions.

I. INTRODUCTION

THE GaInP/GaAs HBT is now well accepted as a serious competitor to the conventional AlGaAs/GaAs HBT. The major interest in GaInP/GaAs HBT's stem from the manufacturing advantages compared to AlGaAs/GaAs HBT's. The latter requires delicate base etch monitoring during fabrication, whereas GaInP/GaAs HBT's can be structured in a highly selective etch process that allows easy and economic fabrication. Excellent dc and RF results have been demonstrated for GaInP/GaAs HBT's [1]–[3]. Low phase-noise Ka-band oscillators have already been realized [4].

Recently, the GaInP/GaAs HBT technology has also been applied to monolithic power amplifiers. Under short pulse conditions (pulse width = 10 μ s, duty cycle = 10%) an amplifier with an output power of 5.3 W and a PAE of 34% at 9.5 GHz and an amplifier with 9.9 W output power and 33% PAE at 8.5 GHz have yet been realized [5], [6].

In this letter, we report on the fabrication and performance of monolithic power amplifiers that are designed for long pulse and CW operation. The MMIC's deliver state-of-the-art performance with respect to efficiency, output power, operation frequency, and pulse conditions of any GaAs-based HBT power amplifier [7]–[9].

II. GAINP/GAAS HBT TECHNOLOGY

The processed 3-in. wafers incorporate an InGaAs cap and a highly carbon-doped base layer with a thickness of 100 nm and a doping level of $5 \times 10^{19} \text{ cm}^{-3}$. The 1- μm -thick GaAs collector is doped at $2 \times 10^{16} \text{ cm}^{-3}$. The dc current gain (β)

Manuscript received July 6, 1995. This work was supported by the German MOD.

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Publisher Item Identifier S 1051-8207(96)00442-4.

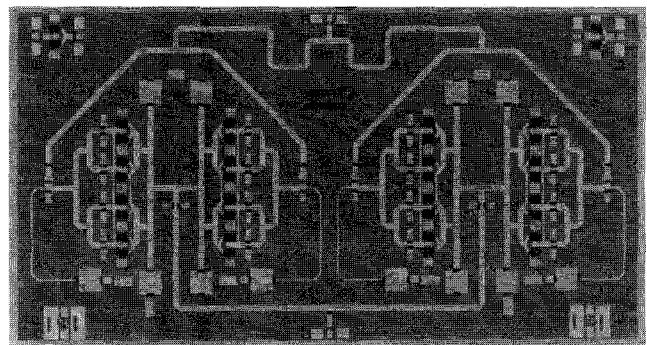


Fig. 1. A photograph of a X-band GaInP/GaAs HBT MMIC power amplifier. The chip size is 8 mm by 4 mm.

is typically 25 resulting in a breakdown voltage (BV_{CEO}) of ~ 20 V.

The HBT process utilizes a conventional mesa approach and a self-aligned base metallization with respect to the emitter stripe. Standard optical contact lithography, selective wet etching, and deep high-dose proton isolation are applied. Nonalloyed TiPtAu is used for the emitter and base contacts. GeNiAu is applied as subcollector contact. The emitter fingers are adequately ballasted with 11Ω per finger to suppress completely the current gain collapse effect. The backsides of the wafers are thinned to a thickness of 100 μm . Subsequently the via-holes are formed for emitter grounding by dry etching.

III. CIRCUIT DESIGN

A photograph of a fabricated single-stage HBT MMIC power amplifier is shown in Fig. 1. The chip incorporates 128 emitter fingers, each having an area of $2 \times 30 \mu\text{m}^2$. The overall emitter area of $7680 \mu\text{m}^2$ allows high output power levels with moderate power and current densities ($j = 2 \times 10^4 \text{ A/cm}^2$). This is an important aspect since there is some evidence that reliability of HBT devices strongly depend on current density [10].

The power amplifier design is based on a temperature-dependent large-signal HBT model fitted to measured small-signal S -parameters as well as dc characteristics. For circuit simulation LIBRATM (HP-EEsof) and an electromagnetic simulator (SONNET software) are used. The amplifier design is checked by Rollet's as well as Nyquist's stability criterion to avoid even and odd mode oscillations.

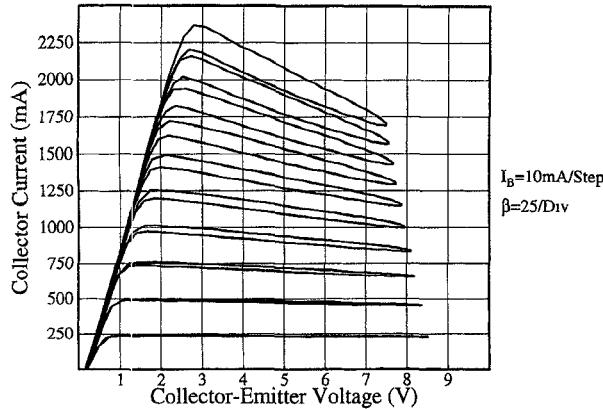


Fig. 2. Measured I - V characteristic of a power amplifier with 16 unit-cells. Each unit-cell has eight emitter fingers with an emitter area of $2 \times 30 \mu\text{m}^2$.

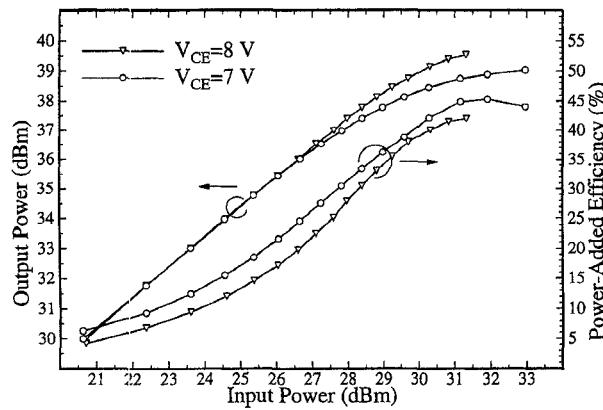


Fig. 3. Output powers and power-added efficiencies versus input power for a typical power amplifier. The curves are traced at different collector biases of $V_{CE} = 7 \text{ V}$ and $V_{CE} = 8 \text{ V}$, respectively ($f = 10 \text{ GHz}$, pulse width = $100 \mu\text{s}$, duty cycle = 10%).

To improve the amplifier stability resistive losses are added to the base bias networks.

IV. CIRCUIT PERFORMANCE

Single-finger HBT's show maximum frequencies of oscillation (f_{\max}) of 130 GHz. The 8-finger HBT power unit-cells have a f_{\max} of 50 GHz and a maximum available gain (MAG) of 13 dB at 10 GHz ($V_{CE} = 8.5 \text{ V}$, $j = 2 \times 10^4 \text{ A/cm}^2$). The unit-cell delivers typically 0.5–0.6 W CW output power with a PAE of 60%. The thermal resistance of the unit-cell at 20°C is estimated to 130 K/W at a power density of 1 W/mm.

Fig. 2 shows a typical on-wafer measured I - V characteristic (measured with a Tektronix 370A curve tracer) of a power amplifier demonstrating the stable dc operation of this amplifier. The series resistance of $\sim 1 \Omega$ is mainly determined by the needle access resistance.

For large-signal analysis the chips are mounted in a test fixture. All measurements are carried out without any external tuning. The power-added efficiencies are calculated considering the power dissipation in the collector terminals as well as the base terminals.

Fig. 3 illustrates the power performance at 10 GHz under long pulse (pulse width = $100 \mu\text{s}$, duty cycle = 10%) conditions. At 7 V collector bias a maximum output power

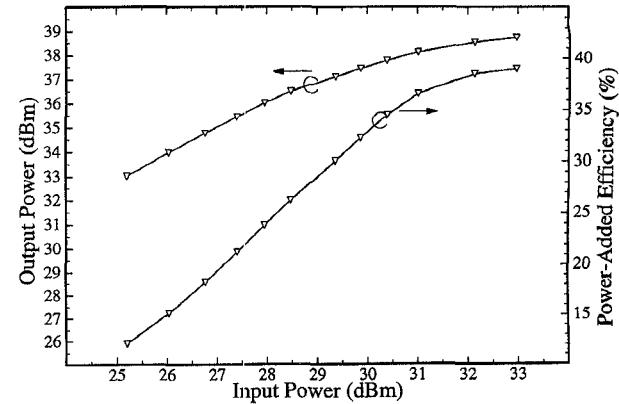


Fig. 4. Measured CW output power and power-added efficiency as a function of input power at 10 GHz of a typical power amplifier. The collector bias is 7 V.

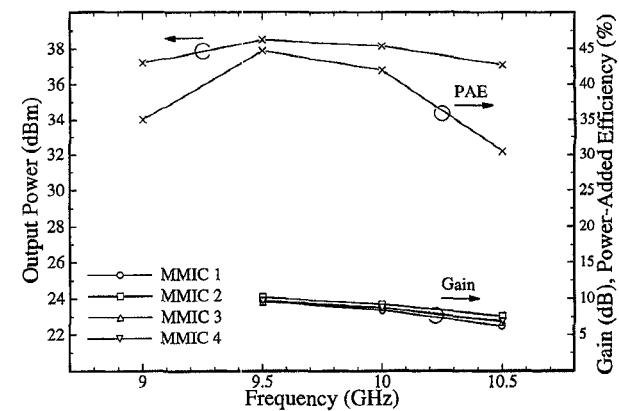


Fig. 5. Output power and PAE versus frequency of a power amplifier at an input power level of 30 dBm. Also shown are measured gains versus frequency of several power amplifiers at an output power of 5 W (pulse width = $100 \mu\text{s}$, duty cycle = 10%, $V_{CE} = 7 \text{ V}$).

of 8 W is reached with a PAE of 44%. The peak power-added efficiency is 45% at 7.7 W with 7 dB gain. At a collector bias of 8 V the amplifier delivers 9 W output power with a PAE of 42% and a gain of 8 dB. Under CW conditions the amplifier delivers 7.5 W, a PAE of 39%, and a gain of 6 dB at 10 GHz (see Fig. 4).

Fig. 5 shows the frequency dependence of output power and PAE for a power amplifier at an input power level of 30 dBm. The highest output powers and efficiencies are obtained between 9.5 and 10 GHz. The variation of gains in the 9–10.5 GHz range for 4 MMIC chips are also shown in Fig. 5. At an output power level of 5 W the gains of the single-stage amplifiers are between 9.5 and 10.5 dB at 9.5 GHz. The decrease of gain at higher frequencies is mainly due to the intrinsic RF behavior of the basic-cell.

Amplifier yields of 50% averaged over several wafers have been obtained demonstrating the high manufacturing level of GaInP/GaAs-based HBT MMIC power amplifiers.

V. CONCLUSION

In conclusion, we have demonstrated high-efficiency and high-power X-band amplifiers based on a well established and optimized GaInP/GaAs heterojunction bipolar transistor

technology. Maximum output powers of up to 9 W and peak power-added efficiencies of 45% have been measured at 10 GHz under critical long pulse conditions.

ACKNOWLEDGMENT

The authors would like to thank S. Heuthe and A. Geyer for technological advice. The continuous support of this work by P. Narozny, H. Dämbkes, and B. Adelseck is gratefully acknowledged. We also appreciate technical cooperation with our colleagues from Thomson-CSF.

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